A 100-Gb/s Real-time Burst-mode Coherent PDM-DQPSK Receiver

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Abstract We demonstrate a 100-Gb/s real-time coherent burst-mode receiver for the first time, based on 32-GSa/s low-profile ADCs. A particularly designed DSP architecture was implemented for rapid burst data recovery, FTL transience compensation and effective channel equalization.

Introduction
With the rapidly increasing bandwidth demand in recent years, the cost and power consumption for transceiving and switching data in optical networks tend to become tremendous and intolerable. All-optical burst networks have re-attracted attention to tackle this challenge by eliminating the costly and power consuming O/E/O conversion and electrical switching at some switching nodes in metro and regional areas\(^1\). With the channel bit rate reaching 100 Gb/s or beyond, coherent technology is desirable to boost the capacity in an optical burst network with reasonably long reach.

Recently, several studies on the coherent burst-mode receiver (BMR) have been reported\(^3\). One representative work realized 112-Gb/s polarization division multiplexing (differential) quadrature phase shift keying (PDM-(D)QPSK) burst-mode transceivers with fast wavelength tuning using offline digital signal processing (DSP)\(^4\). Another work demonstrated 28-Gb/s real-time PDM-QPSK burst-mode receiver\(^5\), in which special header design was employed for polarization demultiplexing, with no chromatic dispersion (CD) or polarization mode dispersion (PMD) compensation implemented. Previously, we have proposed a data-aided (DA) DSP architecture with complete function blocks to support fast and stable data recovery and to alleviate various impairments caused by fiber links, fast tunable lasers (FTLs), etc\(^7\).

In this paper, we implement a 100-Gb/s PDM-DQPSK coherent BMR with real-time DSP based on field-programmable gate arrays (FPGAs). Low-profile 32-GSa/s analog-to-digital convertors (ADCs) are employed, with the worst effective number of bits (ENOB) being only 2.5 bits. Improved DSP architecture is realized, which facilitates rapid burst data recovery despite of FTL transience induced impairments. Optical bursts reception after 500-km transmission is successfully demonstrated. The real-time 100-Gb/s BMR demonstration validated the technical feasibility of 100-Gb/s burst-mode transmission, implying the practicability of high-speed burst transceiving in optical burst metro networks.

Real-time BMR Prototype Implementation

The real-time coherent BMR prototype is composed of an optical frontend, four electrical signal interface modules and a DSP module, as shown in Fig. 1. One of the four interface modules acts as the master which synchronizes and controls the others. Each interface module consists of a low-pass filter (LPF), an ADC, and an FPGA of the 1\(^{st}\) type (FPGA1). The FPGA1 deserializes the high-speed data streams and carries out some pre-processing. Then the tributary electrical signals are fed into the DSP module, which consists of one or multiple FPGAs of the 2\(^{nd}\) type (FPGA2) optimized for the main processing.

![Fig. 1: Real-time BMR prototype implementation](image)

In our demonstration, four commercial 32-GSa/s ADCs were employed. With respect to the 100-Gb/s, 25-Gbaud PDM-DQPSK optical signal, the 32-GSa/s ADCs support at most a 1.28-Sa/sym sampling ratio, which will inevitably cause some degradation in the BMR performance. Furthermore, the four ADC cores interleaved in each ADC were observed to behave differently, resulting in severe

![Fig. 2: ENOB of the ADCs versus analog bandwidth](image)
degradation and fluctuation of the overall ENOB, as shown in Fig. 2. In our demonstration we intended to study the feasibility of such low-profile (and potentially low-cost) ADCs, and no particular action was taken to alleviate this issue.

**Improved DSP Architecture**

![Diagram of DSP architecture](image)

**Fig. 3:** The DSP architecture in the implementation

The improved DSP architecture targeting FPGA implementation is depicted in Fig. 3. The whole DSP is divided into two serial parts implemented respectively in the four FPGA1s and one FPGA2. In the first part, the four digitalized signals from the ADCs are first resampled to 2Sa/Sym in order to mitigate the ADC low sampling impact. Then the deskew and the mean correction algorithms are carried out to compensate the optical frontend imperfection. After that, the four signals are combined together and transferred to the second part where the main coherent receiving algorithm functions are implemented.

In FPGA2, the overall DSP architecture adopts feed-forward structures for smooth pipelining operation. Several designs are incorporated specially for receiving optical burst signals. First, the data-aided rapid framing recovery is realized within tens of symbols. Second, compared with conventional constant modulus algorithm (CMA) suffering from considerable and statistically varying convergence time, the employed data-aided (DA) frequency domain (FD) equalization algorithm guarantees fast and stable channel estimation independently of the actual channel distortions. A 16-tap FD channel equalizer is implemented with the support of repeated 16-symbol channel estimation training sequences, which adaptively compensates the channel distortions such as residual CD, differential group delay (DGD) and polarization dependent loss (PDL). Moreover, particular algorithm is designed for compensating FTL transience induced power/frequency fluctuation after wavelength tuning, enabling fast DSP convergence within a few nanoseconds.

**Experimental Setup**

The experiment setup is sketched in Fig. 4. At the transmitting end, 10 wavelength division multiplexing (WDM) channels including 1 burst-mode signal channel and 9 other continuous-mode neighbor channels were generated. The burst-mode signal channel employed a digitally sampled distributed Bragg reflector (DS-DBR) FTL with 100-ns tuning time, which was switched alternatively between 1550.116 nm and 1550.516 nm for each burst. The average stable linewidth of the FTL is around 1 MHz. Each burst contained 99156 symbols including an 1152-symbol header (overhead<1.2 %) and lasted for about 4 μs. The effective burst guard time can be adjusted by inserting some dummy symbols before the burst header. The measured optical signal in the 1550.116-nm burst channel and the measured WDM spectra before and after the interleaver are shown in Fig. 4 insets.

For the transmission link, a recirculating loop consisting of 80-km or 100-km single-mode fiber (SMF) span equipped with erbium doped fiber amplifier (EDFA) and polarization scrambler (PS) was built for multi-scenario tests. A noise loading module and a 0.4-nm optical filter were placed in front of the receiver for adjusting the received optical signal-to-noise ratio (OSNR).

At the receiver side, an Agilent external cavity laser (ECL) with a linewidth less than 100 kHz was used as the local oscillator (LO). The optical burst signal was fed into our BMR prototype for real-time signal reception. Alternatively, the mixed and detected signals were captured by a Tektronix 50-GSa/s real-time oscilloscope (OSC) and processed either
offline or in our FPGAs for comparative studies.

Results and Discussion
The DSP convergence was studied, and the results are plotted in Fig. 5. First, a number of dummy symbols were inserted in front of the burst header, resulting in a 400-ns effective guard time which was much more than adequate for the FTL wavelength tuning and the DSP convergence. The corresponding BER curve thus serves as the comparison baseline. Then the effective guard time was decreased to 120 ns and the BER was measured again. Negligible penalty was observed by significantly decreasing the guard time. Since nearly 100 ns out of the 120 ns was for the wavelength tuning of the FTL, it can be deduced that the burst receiving algorithm converged within 10–20 ns.

![Fig. 5: BER performance at different guard times.](image)

![Fig. 6: BER performance in different scenarios.](image)

![Fig. 7: BER performance versus PDL and DGD.](image)

Transmission experiments for a few offline and real-time scenarios were conducted and the BER versus OSNR performances are shown in Fig. 6. The PDM-QPSK theoretical curve, and the back-to-back continuous-mode BERs using Agilent ECLs for both the transmitter and the LO and using float-point offline time-domain equalization (TDEQ), are plotted as comparative baselines. When using FTL in the burst transmitter, the blind TDEQ did not work any more while our FA FDEQ based BMR received the bursts successfully. Our fixed-point offline DSP induced about 2-dB penalty compared with the blind TDEQ baseline at the hard-decision forward error correction (HD-FEC) threshold. About 1 dB out of this penalty was introduced by the large dynamic linewidth and phase noise of the FTL as well as the differential encoding utilized for preventing the phase noise induced cycle slip. The other around 1-dB penalty was attributed to the limited length of training sequence in the FDEQ and the fixed-point and parallelized realization of the DSP. When using the real-time BMR for the burst reception, around 4-dB further penalty was induced for back-to-back case and a little more penalty after 500-km transmission. The large penalties were mainly due to the poor ENOBs of the used ADCs. The worst case of only 2.5-bit ENOB in slave module 2 severely degraded the receiver performance when the four tributary signals mixed together in the equalizer.

The real-time BMR performance with respect to DGD and PDL were also studied. The burst signals with different DGDs or PDLs were generated separately, and corresponding digital data were fed into and processed by the real-time DSP. It is observed that the BER of the recovered burst data kept stable with a DGD variance up to 25 ps for both 0 and 45 degree input polarization angles. Also, the BERs degraded slightly as the PDL increased to 2 dB. These demonstrated the FDEQ based DSP had good tolerance against DGD and PDL.

Summary
We have experimentally demonstrated a 100-Gb/s real-time burst mode PDM-QPSK receiver for the first time, based on low-profile ADCs with the worst ENOB of 2.5 bits. An innovative DA DSP architecture was proposed and implemented, with feed-forward structures and FTL transience compensation. Successful optical bursts real-time reception was achieved after 500-km transmission, validating 100-Gb/s BMR feasibility using low-profile and potentially low-cost ADCs for optical burst metro networks.

References
[6] F. Vacondio et al., ECOC 2012, Tu.3.A.1